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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/410,928	10/01/1999	ANDREW M. JONES	99-TK-254	7656

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EXAMINER	
PEUGH, BRIAN R	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/410,928	JONES ET AL.
	Examiner	Art Unit
	Brian R. Peugh	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,7,9,10,13,15 and 17-19* is/are rejected.

7)☒ Claim(s) *3,4,6,8,11,12,14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed June 24, 2004, in response to Examiner's Action of May 25, 2004. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-19 have been presented for examination in this application. In response to Applicant's Amendment of June 24, 2004, claims 1, 6, 8, 14, 16, 17, and 18 have been amended.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "a transaction-based bus which defines a cache coherency transaction within its transaction set" (claim 17, lines 2-3) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 6, 17, and 18 are objected to because of the following informalities:

Regarding claim 6, line 5: Remove "main" in order to facilitate proper antecedent basis.

Regarding claim 6, lines 8-9: Replace both instances of "main memory" with –the memory system-- in order to facilitate proper antecedent basis [claim 5, line 3].

Regarding claim 17, the Examiner believes that the phrase "...when the cache memory is not coupled to the transaction-based bus" of lines 8-9 is meant to refer to when the cache memory is not *directly* coupled to the transaction-based bus, according to Applicant's Arguments of April 26, 2004 [page 7, section A., para. 2]. The Examiner will interpret the claim as such, and encourages the Applicant to amend the claim in order to better detail the claimed invention.

Claim 18 is objected to as being dependent upon a previously objected claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 9, 10, 17, 18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Stamm (US# 5,432,918).

Regarding claim 1, Stamm teaches **a computer system comprising: a memory system where at least some of the memory is designated as shared memory** [memory (12); col. 4, lines 22-26]; **a transaction-based bus coupled to the memory system wherein the transaction-based bus includes a cache coherency transaction defined within its transaction set** [Fig. 1; bus (11); col. 7, lines 43-48; CPU(10) inherently stores transaction that are to be 'initiated']; **a processor having a cache memory, the processor coupled to the memory system through the transaction based bus** [col. 3, lines 28-32; col. 4, lines 11-15; Fig. 1, backup cache (15) or primary cache (14)]; **a plurality of system components other than the processor coupled to the transaction-based bus, wherein the system components**

access the memory system directly through the transaction based bus, but do not access the cache memory directly through the transaction based bus [CPUs (28); Fig. 1; col. 4, lines 22-26]; **a request issued by one of the plurality of system components and addressed to the processor, wherein the request indicates a request to perform a cache coherency operation** [data read; col. 7, lines 10-16], **and wherein the processor is configured to respond to the request** [data read] **by treating the request as an explicit command to perform the cache coherency operation** [data read, which necessitates the write-back to memory (12) operation to first be performed].

Regarding claim 2, Stamm teaches **the request is implemented independent of any interrupt mechanism in the processor** [Stamm does not teach that an interrupt is necessary to implement the request, according to col. 7, lines 10-16].

Regarding claim 9, Stamm teaches **a method for managing cache coherency in a shared memory system wherein the shared memory system is shared by a plurality of modules** [system memory (12)]; modules refer to CPUs (10) & (28); Fig. 1; col. 4, lines 20-26], **including a processing unit** [CPUs (10) & (28)], **and wherein the plurality of modules, including the processing unit, are coupled to a system bus** [Fig. 1; col. 4, lines 20-25], **the method comprising the steps of: causing the processing unit to cache at least some locations of the shared memory system in a cache memory** [col. 3, lines 39-45]; **initiating a cache coherency transaction on the system bus using one of the plurality of modules other than the processing**

unit; and in response to the cache coherency transaction, causing the processing unit to execute a cache coherency operation [col. 7, lines 10-16 & 43-48].

Regarding claim 10, Stamm teaches **the step of initiating is performed without using an interrupt mechanism of the processing unit** [Stamm does not teach that an interrupt is necessary to implement the request, according to col. 7, lines 10-16].

Regarding claim 17, Stamm teaches **a computing device comprising: a transaction-based bus** [Fig. 1; bus (20) or bus (11)] **which defines a cache coherency transaction within its transaction set** [col. 7, lines 43-48; CPU(10) inherently stores transaction that are to be 'initiated']; **a processor coupled to the transaction based bus** [col. 3, lines 28-32; col. 4, lines 11-15], **a cache memory coupled to the processor, but not coupled directly to the transaction-based bus** [Fig. 1; backup cache (15) or primary cache (14)]; **and wherein the cache coherency transaction is defined within the transaction-based bus even when the cache memory is not** [directly] **coupled to the transaction-based bus** [Fig. 1; col. 7, lines 43-48].

Regarding claim 18, Stamm teaches **a plurality of system components other than the processor** [CPUs (28); Fig. 1], **wherein the plurality of system components are coupled to the transaction-based bus** [system bus (11)], **wherein the plurality of system components other than the processor can initiate a cache memory operation** [data read; col. 7, lines 10-16] **by using the cache coherency**

transaction defined within the transaction-based bus [col. 7, lines 43-48], **wherein the processor is configured to respond to the cache coherency transaction** [data read] **by treating the cache coherency transaction as an explicit command to perform a cache coherency operation** [write-back to memory (12)].

Regarding claim 19, Stamm teaches **the plurality of system components other than the processor are selected from the group consisting of: an external memory interface** [col. 4, lines 20-22], **a PCI bridge, peripheral subsystem interface, and direct memory access controller.**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 7, 13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stamm (US# 5,432, 918) as applied to claims 1, 2, 9, 10, 17, 18, and 19 above, and further in view of Farrall et al. (US# 2002/0007442).

Regarding claim 5, Stamm fails to teach that teaches the cache coherency transaction comprises a cache flush transaction and the request includes an address in the shared memory to be flushed from the cache. Farrall et al. teaches **the cache**

coherency transaction comprises a cache flush transaction and the request includes an address in the shared memory to be flushed from the cache [para. 82, 84 & 85].

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Stamm and Farrall et al. before him at the time the invention was made to modify the cache coherency system of Stamm to include the flush coherency mechanisms of Farrall et al., because then it is not necessary to request the cache coherency operation to be executed on a particular address stored in the cache, as taught by Farrall et al. [para. 18].

Regarding claim 7, Farrall et al. teaches **the cache coherency transaction comprises a cache purge transaction and the request includes an address in the shared memory to be purged from the cache** [para. 82 & 87-89].

Regarding claim 13, Farrall et al. teaches **the cache coherency transaction comprises a cache flush transaction and the step of initiating indicating an address in the shared memory to be flushed from the cache memory** [para. 82, 84 & 85].

Regarding claim 15, Farrall et al. teaches **the cache coherency transaction comprises a cache purge transaction and the step of initiating includes indicating an address in the shared memory to be purged from the cache memory** [para. 82 & 87-89].

Allowable Subject Matter

Claims 3, 4, 6, 8, 11, 12, 14, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to related a related caching system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 17, 2004

Brian R. Peugh
Patent Examiner
Art Unit 2187